REMARKS

Claims 1-13 are pending in the application; the status of the claims is as follows:

Claims 1, 2, 4, 5, and 7-12 are rejected under 35 U.S.C. § 102(a) as being anticipated by PCT Published Application No. WO98/40874 A1 to Takebe ("Takebe").

Claims 3, 6, and 13 are objected to as being dependent upon a rejected base claim, but allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35 U.S.C. § 102(a) Rejection

The rejection of claims 1, 2, 4, 5, and 7-12 under 35 U.S.C. § 102(a) as being anticipated by Takebe, is respectfully traversed because the reference fails to disclose each element of the subject claims.

Takebe discloses an apparatus for displaying an interlaced image on a non-interlaced screen, such as displaying an image from an NTSC system on a VGA computer monitor. Column 1, lines 15-27. The analog main image signal, VD_M, is converted to image data by A/D converter 103, which image data is then provided to selector 104. Similarly, analog sub-image signal, VD_S, is converted to image data by A/D converter 106 and stored to frame memories 107a/b. The image data from frame memories 107a/b is then sent to selector 104. Selector 104 selects data from either frame memories 107a/b or A/D converter 103 for display. Synchronous detection circuit 102 and synchronous separation circuit 105 extract horizontal and vertical synch signals from the main-image and sub-image, respectfully. Synthesis controller 110 orchestrates operation of the circuitry based on configuration registers programmed by CPU 101.

It is respectfully submitted that Takebe fails to disclose any processing of the image data. Rather, the Takebe circuitry merely selects either main image data or sub-image data to pass through to the display device.

It is also respectfully submitted that synchronous detection circuit 102 and synchronous separation circuit 105 do not process image data. Rather, these circuits merely extract or separate the horizontal and vertical synch (timing) pulses contained within the analog image signals.

It is also respectfully submitted that memories 107a/b are not asynchronous circuitry for processing a portion of the image data. Indeed, Takebe fails to disclose that memories 107a/b do anything other than merely store image data.

Thus, with respect to claim 1, Takebe fails to disclose "synchronous type processing means for carrying out a first image process on image data that is the subject of processing" and "asynchronous type processing means for carrying out a second image process on image data of a predetermined region of said image data that is the subject of processing."

With respect to claim 2, it is submitted that Takebe fails to disclose either synchronous or asynchronous type processing means as provided above with regard to claim 1. Even assuming *arguendo* that Takebe discloses synchronous processing means, the reference fails to disclose "a memory in which an output of said synchronous type processing means is stored." The Office Action alleges that memories 107a/b read on this claim element. However, Takebe does not disclose a signal path from the alleged synchronous processing means to the alleged memory, *i.e.*, from circuits 102/105 to frame memories 107a/b. The outputs of circuits 102/105 merely provide reset signals to various counters in synthesis controller 110. *See* Figs. 7 and 8. Thus, Takebe fails to disclose "a memory in which an output of said synchronous type processing means is stored." Moreover, the main image data is not stored to a memory and subsequently replaced by the sub-image data. Therefore, Takebe fails to disclose "replacement means for replacing

a portion of an output of said synchronous type processing means *stored in said memory* with an output of said asynchronous type processing means."

With respect to claim 4, it is submitted that because Takebe fails to disclose processing of any image data, it fails to disclose "a first image processor formed of a hardware circuit, and carrying out a first image process on input image data," as well as "a second image processor carrying out a second image process on a fragment of said input image data according to a program of predetermined software." Moreover, because Takebe fails to disclose a memory in which the combination of the main-image and sub-image is stored, it fails to disclose "a memory in which image data subjected to said first image process and image data subjected to said second image process are synthesized and stored."

With respect to claim 5, it is submitted that Takebe fails to disclose a memory in which the image data subject to a first image process is stored and then overwritten in part by the image data subject to a second image process. Accordingly, Takebe fails to disclose that "data of said memory in which image data subjected to the first image process is stored is overwritten by image data subjected to the second image process."

With respect to claim 7, Takebe fails to disclose software-based image processing. Accordingly, Takebe fails to disclose that "said software is rewritable."

With respect to claim 8, Takebe fails to disclose that the sub-image comes from the main-image or that the main-image is analyzed to identify the portion of the main-image that comprises the sub-image. Therefore, Takebe fails to disclose that "said second image processor detects a region on which the second image process is to be carried out by scanning input image data."

With respect to claim 9, Takebe fails to disclose performing any image processing on any image data and, therefore, fails to disclose "carrying out a first image process on

input image data through a hardware circuit," or "carrying out a second image process on a fragment of the input image data through software."

With respect to claim 10, Takebe fails to disclose that the image data is analyzed to identify a region for image processing. Accordingly, Takebe fails to disclose" detecting a region on which the second image process is to be carried out by scanning input image data, and carrying out the second image process on the detected region."

With respect to claim 11, Takebe fails to disclose a synchronous-type processor, an asynchronous-type processor, or any processing of any image data. Accordingly, Takebe fails to disclose either "a synchronous-type data processing device for carrying out a first image process on image data that is the subject of processing," or "an asynchronous-type data processor for carrying out a second image process on image data of a predetermined region of said image data that is the subject of processing."

With respect to claim 12, Takebe fails to disclose either "a memory for storing an output of said synchronous-type processing device," or replacing "a portion of an output of said synchronous-type processing device stored in said memory with an output of said asynchronous-type processor."

Accordingly, it is respectfully requested that the rejection of claims 1, 2, 4, 5, and 7-12 under 35 U.S.C. § 102(a) as being anticipated by Takebe, be reconsidered and withdrawn.

CONCLUSION

Wherefore, in view of the foregoing remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

Any fee required by this document other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be construed as also constituting a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any other fee required for such Petition for Extension of Time and any other fee required by this document pursuant to 37 C.F.R. §§ 1.16 and 1.17, other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

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